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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,423	09/29/2000	Steve Morley	1956/130	3866

2101 7590 04/28/2004

BROMBERG & SUNSTEIN LLP
125 SUMMER STREET
BOSTON, MA 02110-1618

EXAMINER	
NAMAZI, MEHDI	

ART UNIT	PAPER NUMBER
2188	12

DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/675,423	MORLEY ET AL.	
	Examiner	Art Unit	
	Mehdi Namazi	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-100* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-100* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to amendment filed January 12, 2004.

Claims 101-130 have been canceled. Claims 1-100 are pending in the application.

Response to Arguments

1. Applicant's arguments with respect to claims 1-100 have been considered but are moot in view of the new ground(s) of rejection.

Specification

1. The disclosure is objected to because of the following informality: the serial number and patent number of related applications are still missing on page 2. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 4, 8, 11, 14-21, 24-27, 29, 33, 36, 39-45, 49-52, 54, 58, 61, 64-70, 74-77, 79, 83, 86, 89-96, 99, 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning (U.S. Patent No. 6,148,368), and further in view of Yoo et al. (U.S. Patent 5,866,451).

As per claims 1, 26, 51, 76, DeKoning teaches a system for storing data, the system having one or more devices (fig. 2, elements 224, 210), the system comprising:

A first cache level for caching data from sender into first level cache (col. 8, lines 59-65)(cache segments 225 and 226 is consider as first level cache, which receive data from element 217);

A second cache level for caching data from first cache level into a log structure (col. 8, lines 65-1, and col. 9, lines 16-21)(data are written into segments 235, 236, and 237, from first level cache, where 235, 236, and 237 are associated with log structure); and a storage level for storing data from CL into a second random – access structure, wherein CL is the first cache level or the second cache level (col. 9, lines 1-2, where main disk region 234 is consider as a storage level, and data from segments 235, 236, or 237 which consider as second level moves to storage level or 234).

Dekoning teaches the claimed invention as detailed above in the previous paragraph, but fails to teach that the first level cache is a random – access structure.

Yoo teaches a method of making a semiconductor device wherein the first level cache is a SRAM(Static **Random Access** Memory) (col. 2, lines 15-19).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a SRAM as first level cache memory, as thought by Yoo into system of DeKoning in order to speed up read and write to the memory.

As per claims 2, 8, 11, 27, 33, 36, 52, 58, 61, 77, 83, and 86, DeKoning teaches the log structure includes one or more segments, segment elements, or segment blocks (fig. 2, elements 225, 226, 228).

As per claims 4, 29, 54, and 79, DeKoning teaches wherein the log structure further includes a segment summary, the segment summary tracking information

regarding the configuration of at least one segment in the log structure (fig. 5, elements 235 and 236, shows each segment is holding log data summary for each segment).

As per claims 14, 39, 64, 89, 102, 112, and 122, DeKoning teaches the first cache level is a memory – based cache (fig. 2, elements 225, 226, 228, are all cache memory).

As per claims 15, 17, 40, 42, 65, 67, 90, 92, DeKoning teaches the first and second cache levels are a write-back cache (col. 8, lines 30-33).

As per claims 16, 41, 66, 91 DeKoning teaches the second cache level is a disk – based cache (fig. 2, elements 235, 236, and 237 are cache memories).

As per claims 18, 19, 43, 44, 68, 69, 93, 94, DeKoning teaches the second cache level further caches the log structure parity data for the data cached in the log structure, and the storage level stores in the second random – access structure parity data for the data stored in the second random – access structure (fig. 2, element 228 shows a parity segment which been used from first level to the second cache level to the storage level).

As per claims 20, 21, 45, 46, 70, 71, 95, 96, DeKoning teaches wherein the log structure, and second random – access structure are configured as a Redundant Array of Independent Disks structure (col. 3, lines 46-57).

As per claims 24, 49, 74, 99, DeKoning teaches wherein one or more storage devices are disks (fig. 2, element 234).

As per claims 25, 50, 75, 100, DeKoning teaches wherein the one or more storage devices are a disk array (fig. 2, elements 232).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3, 6, 7, 9, 10, 12, 13, 28, 31, 32, 34, 35, 37, 38, 53, 56, 57, 59, 60, 62, 63, 78, 81, 82, 84, 85, 87, and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning, and Yoo, and further in view of Courtright, II et al. (Courtright)(U.S. Patent No. 6,105,103).

As per claims 3, 9, 12, 28, 34, 37, 53, 59, 62, 78, 84, and 87, Dekoning, and Yoo teach the claimed invention as detailed above in the previous paragraph, but fails to teach that the log structure further includes a segment database, the segment database tracking information regarding the configuration of user data stored in at least one segment in the log structure.

Courtright teaches a disk array with plurality of segments, where user data block is found in the log segment (col. 12, lines 2-3). In this way Courtright teaches a disk array with plurality of segments with users data, in order to control unanticipated activities.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a segment of plurality of segments in disk array

for information with regard to users data, as thought by Courtright into system of DeKoning in order to control access to system and unanticipated activities.

As per claims 10, 13, 35, 38, 60, 63, 85, and 88, DeKoning teaches wherein the segment database is stored in at least one segment element, or segment block (figs. 5, and 6).

As per claims 6, 7, 31, 32, 56, 57, 81, 82, Dekoning teaches the claimed invention as detailed above in the previous paragraph, but fails to teach that the log structure further includes one or more logical - to - physical maps, the logical - to - physical maps tracking information regarding the location of user data stored in at least one segment in the log structure, and the map elements tracking information regarding the location of contiguous user data stored in at least one segment in the log structure. .

Courtright teaches a paged addressing method for dynamically addressed storage subsystem, which stores the logical to physical address map of each segment in LDMC cache (abstract, lines 1-2, and fig. 2B, element 45).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a LDMC cache to track logical to physical address of user data for any changes in configuration.

4. Claims 5, 22, 30, 47, 55, 72, 80, and 97 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning, and Yoo, and further in view of Mittal (U.S. Patent No. 5,829,025).

As per claims 5, 30, 55, and 80, Dekoning, and Yoo teach the claimed invention as detailed above in the previous paragraph, but fails to teach that the log structure

further includes a bit map, the bit map tracking information regarding live user data stored in at least one segment in the log structure.

Mittal teaches computer system of allocating cache memories in a multilevel cache hierarchy, where two bits would be allocated in the instructions for identifying the particular classification at each cache level (col. 10, lines 16-18). In this way Mittal teaches two different bits, where each bit is used for different instructions.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use different bits for different instructions as thought by Mittal into system of Dekoning, and Yoo in order to use first bit out of two to provide the locality hint value for L1 cache, and second bit to provide locality hint value for L2 cache (col. 8, lines 30-33).

As per claims 22, 47, 72, and 97, Dekoning, and Yoo teach the claimed invention as detailed above in the previous paragraph, but fails to teach that the storage capacity of the first cache level is smaller then the storage capacity of the second cache level.

Mittal teaches computer system of allocating cache memories in a multilevel cache hierarchy, where L2 (level 2) cache is larger then L1 (level 1) cache (col. 9, lines 42-43). In this way Mittal teaches a hierarchy cache, where L1 cache is smaller then L2 cache since it is closer to processor and faster then L2 cache.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a smaller cache as L1 cache in cache hierarchy as thought by Mittal into system of Dekoning, and Yoo in order to speed up access to data for feeding processor.

5. Claims 23, 47, 48, 72, 73, 97, 98, are rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning, and Yoo, and Mittal.

As per claims 23, 48, 73, 98, DeKoning, Yoo, and Mittal do not specifically disclose that the storage capacity of the second cache level is at least 10% of the storage capacity of the one or more storage devices, such limitations are merely a matter of design choice and would have been obvious in the system of DeKoning, Yoo, and Mittal. The limitations in above claims do not define a patentably distinct invention over that in DeKoning, Yoo, and Mittal since both the invention as a whole and DeKoning, Yoo, and Mittal are directed to specific number of memories with certain capacity. The division of memory into certain segments with specific capacity for invention as a whole and presents no new or unexpected result, so long as the memory is able to save data. Therefore, to have memory divided into segments in DeKoning, Yoo, and Mittal would have been a matter of obvious design choice to one ordinary skill in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is 703-306-2758. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Mehdi Namazi
Examiner
Art Unit 2188

April 12, 2004

JACK A. LANE
PRIMARY EXAMINER